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Design Modification Approaches of Double-Tail Comparator using Power Gated Techniques: A Review

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Abstract: This article basically prepared to design a low power and a high performance dynamic latch comparator. Nowadays, the need for ultralow-power, area efficient and high-speed analog-to-digital converters is pushing toward the use of dynamic regenerative comparators to maximize speed and power efficiency. Based on the presented analysis, a new dynamic comparator is proposed, where the circuit of a conventional double tail comparator is modified for low-power and fast operation even in small supply voltages.The proposed design has been simulated on Tanner EDA at 180nm TSMC and achieved up to 15% reduction in power and 71% reduction on kickback noise from the conventional designs and based on the present results and analysis. Comparator is especially designed for open loop configuration without any feedback. Hence, it is the second most widely used device in electronic circuits after Opamp. Comparators are mostly used in analog-to-digital converter. Also, this paper presents a bibliographical survey of recently-published research on different current comparator topologies for low-power and high-speed applications. This paper will help the practicing engineers/ beginners in this field, able to know what are the significant parameters to design low power dynamic latched comparator and its use in various applications.

Keywords: dynamic latch comparator, power consumption, offset voltage, Double-tail comparator, Flash ADCs, CMOS, Tanner EDA

I. INTRODUCTION

In electronics, Operational amplifier (Op-amp) is designed to be used with negative feedback. It can be also used as comparator in open loop configuration. On the other hand, Comparator is especially designed for open loop configuration without any feedback. Hence it is the second most widely used device in electronic circuits after Op-amp. Comparators are known as 1-bit analog-to-digital converter and for that reason they are mostly used in large abundance in A/D converter. In the analog-to-digital conversion process, it is necessary to first sample the input. This sampled signal is then applied to a combination of comparators to determine the digital equivalent of the analog signal. The conversion speed of comparator is limited by the decision-making response time of the comparator. Apart from that, comparators are also can be found in many other applications like zero-crossing detectors, peak detectors, switching power regulators, data transmission, and others. Comparison between two binary numbers is widely used in computer systems and device interfaces for equality. A circuit that compares two binary numbers and decides whether they are equal or not is called comparator [1]. Comparators are known as 1-bit analog to digital converter and for that reason they are mostly used in large abundance in A/D converter. The basic functionality of a CMOS comparator is used to find out whether a signal is greater or smaller than zero or to compare an input signal with a reference signal and outputs a binary signal based on comparison. Many high-speed ADCs, such as flash ADCs, require high-speed, low-power comparator. Due to high speed, low power consumption, high input impedance and full-swing output dynamic latched comparators are very attractive. They use positive feedback mechanism with one pair of back-to backcross coupled inverters (latch) in order to convert a small input-voltage difference to a full-scale digital level in a short time. Designing high-speed comparators suitable to be operable in low supply voltages is a more challenging work. A comparator with a modified latch [2] is different from the conventional circuit by replacing a new latch for low power supply voltage operation (i.e.) for supply voltages down to 0.65V for 65nm technology. This latch is helpful in low power supply voltage operation. A low power, low voltage Successive Approximation Analog-to-Digital Converter (SAR ADC) design based on supply boosting technique is proposed in [3]. SBT is suitable for mixed-signal circuit designed for energy limited applications and systems in where supply voltage is in the order of threshold voltages of the process. Many researches contribute in analyzing the performance of the dynamic comparators. Random decision errors are analyzed in the dynamic comparators using LPTV (Linear

Periodically Time Varying) model [4].

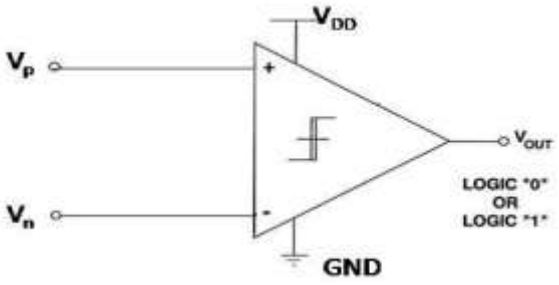

Fig.1. Schematic symbol of comparator

Figure 1 shows the schematic symbol of the comparator VP is the input voltage (Pulse voltage) applied to the positive input terminal of comparator and Vn is the reference voltage (constant DC voltage) applied to the negative terminal of comparator. It is important for the comparator to pass quickly through the transition region of the analog signal.

The comparator consists of three stages*:*

i. Input preamplifier stage

ii. Latch stage

iii. Output buffer stage

The preamplifier stage consists a differential amplifier with active loads. The preamp stage amplifies the input signal to improve the comparator sensitivity. It increases the minimum input signal with which the comparator can make a decision and isolates the input of the comparator from switching noise coming from the positive feedback stage. It also can reduce the input referred latch offset voltage. The positive feedback latch stage is used to determine which of the input signals is larger and amplifies their difference. The output buffer stage consists of a self-biased differential amplifier followed by an inverter which gives the digital output. It converts the output of the latch stage to a full scale digital level output (logic 1 or logic 0). The output buffer stage should accept a differential input signal and not have slew-rate limitations.

II. COMPARATOR ARCHITECTURES

1. **Open loop comparator:**Open-loop, comparators are an operational amplifier without frequency compensation in comparator design to obtain the largest possible bandwidth and good frequency response, hence improving its time response. Since linearity of the design and the precise gain are of no interest in comparator design, no-compensation does not pose a big problem. However, due to its limited gain-bandwidth product, open-loop comparators are too slow for many designing applications. The gain-bandwidth product of cascaded of open-loop comparator usually larger than a single-stage amplifier with the same gain. The implementation design costs more area and large power consumption, and cascading does not give any practical advantages for different types of applications.
2. **Regenerative comparator:** The second architecture of comparator is Regenerative comparators (latches) use positive feedback to accomplish the comparison of two different analog signals. In the Figure 2 shows basic NMOS latch and PMOS latch type. Latches have a faster switching speed and the propagation delay.

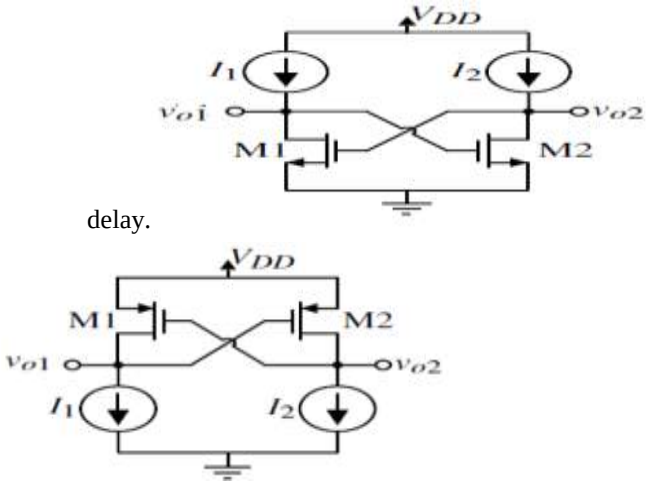

Fig 2. NMOS and PMOS Latch

3.High speed comparator: High speed comparator consists of regenerative comparator as well as open loop comparator. It mainly consists of three building blocks of comparator, Input stage, a flip-flop and S-R latch. It uses a preamplifier to build up the input change to a sufficiently large value of signal and then applying it to the 2nd stage latch. This architecture combines the best aspects of comparator with a negative exponential rise due to preamplifier stage at beginning and positive exponential rise due to latch stage. The main advantages of high speed comparator have a lower propagation delay and faster response time.

4.**Dynamic Latch comparator:** Today's most important comparator design technique is dynamic latch. Dynamic latch is defined as the memory unit that stores the charge on the gate capacitance of the inverter. A dynamic latch is shown in Figure 3. This latch circuit is driven by a clock. During one phase of the clock (clk =1) when the transmission gate is

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closed, the latch acts transparent, and the inverter is directly connected to the input. In the other phase of the clock (clk =0), the transmission gate opens and the inverter's output is determined by the node. The Setup and hold times of comparator is determined by the transmission gate must be taken in consideration in order to ensure proper operation of the latch i.e. adequate level of voltage is stored on the gate capacitance of the latch

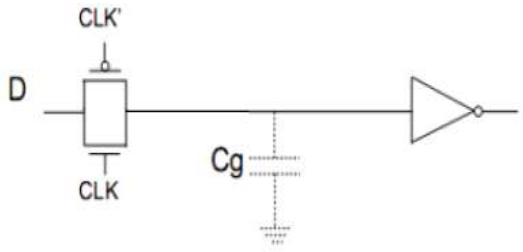

Fig 3.

Dynamic latch

Double-tail Dynamics Compartor :

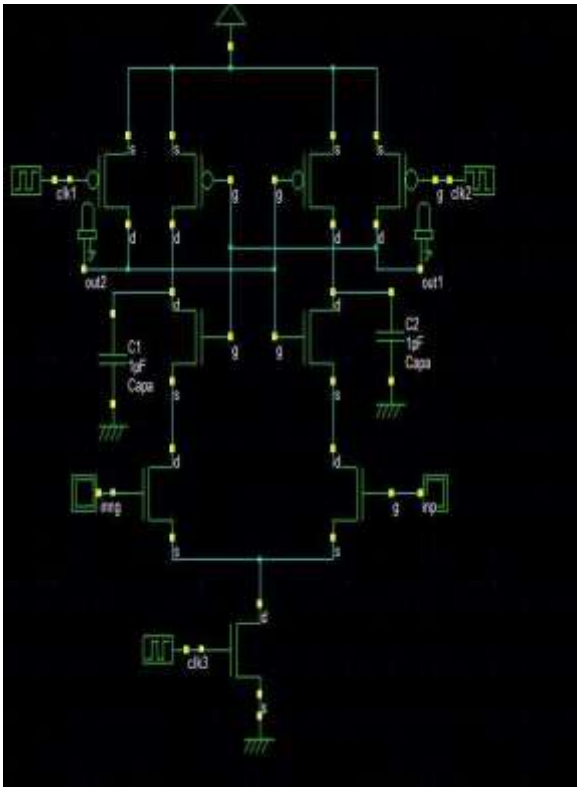

Fig 4. Schematic diagram of the conventional double-tail dynamic comparator

A conventional double-tail comparator is shown in Fig. 3. This topology has less stacking and therefore can operate at lower supply voltages compared to the conventional dynamic comparator. The double tail enables both a large current in the latching stage and wider *M*tail2, for fast latching independent of the input common-mode voltage (*V*cm), and a small current in the input stage (small *M*tail1), for low Offset.

III. BASIC PARAMETER TO DESIGN DYNAMIC LATCH COMPARATOR

Accuracy (offset, noise, resolution)
Settling time (tracking BW, Regeneration speed)
Sensitivity (gain)
Metastability (any decision is better than no decision)
CMRR
Power consumption

An amplifier is employed before the latched comparator, which decreases the offset voltages caused by the device mismatch. To achieve high gain to the output signal of the amplifier, a transmission gate can be utilized between the preamplifier and the latch, which in turn controls the signal path by using the insertion trend. Conventionally, a latch proceeded by preamplifier stages is utilized to employ a faster and accurate comparator [5]. As a result, more area and power are dissipated by employing the preamplifier stages that also border the frequency bandwidth of the input signal. Miyahara et al. proposed a dynamic comparator with a selfcalibration feature based on output averaging [6]. Moreover, in this design, a charge pump is required to regulate the corresponding input-referred offset voltage, making the approach inefficient. However, the involvement of this charge pump circuit limits its accuracy. Nevertheless, convoluted timing necessities and a high number of offset annulment capacitors limit using this comparator in high-speed applications [7].

IV. CHALLENGES IN LOW POWER DESIGN

The basic need for lower power systems is being driven by many market segments. Unfortunately designing for low power circuit another dimension in circuit to the already complex design problem; the design has to be optimized by mainly three parameters for Power, Performance and Area. To conclude this discussion, to summarize the major challenges is that, we have to be addressed if we want to keep power dissipation within this bounds in the next generations of the designing of digital integrated circuits.

- A low supply voltage and circuit design technique, targeting the supply voltages are taken around 1 Volt or lower than 1V and operating with reduced thresholds voltage.

- Low power interconnect, using reduced activity or advanced technology, reduced swing approaches.
- Dynamic power management techniques, are varying with the supply voltage and the execution of design speed according to activity measurements. This can be achieved by the whole design should be divided into sub-circuits whose energy levels also can be independently controlled and by powering down sub-circuits which are not in used.

So, basically here in our work, A new low power, high performance comparator is being proposed, where the circuit of a dynamic double-tail comparator with power gating technique is modified for low-power and fast operation even in small supply voltages. Without any difficulties in circuit design and by adding few transistors, the positive feedback during the regeneration is strengthened, which results in remarkably reduced delay time. Post-layout simulation results in a 180nm CMOS technology provided the analysis results effectively. It is shown that in the proposed dynamic comparator both the power consumption, delay time, kickback noise is significantly reduced.

V. RELATED STUDY

In [8], Nathiya et.al has presented a low-offset dynamic comparator using new dynamic offset cancellation technique is proposed. The technology scaling of MOS transistors enables low voltage and low power which decreases the offset voltage and delay of the comparator. The new technique achieves low offset and low voltage without pre-amplifier. Furthermore, the overdrive voltage of the input transistor can be optimized to reduce the offset voltage of the comparator independent of the input common mode voltage. The input transistor drains nodes and use of buffers at the output nodes can further reduce the offset. The modifications made to the typical differential pair dynamic comparator will be reducing the overall offset voltage. Moreover, the proposed comparator has an advantage thatthe offset voltage does not change by increasing the input common mode voltage compared with the conventional comparator. By implementing this in dynamic comparator technique a low voltage and offset voltage can be achieved.

In paper[9], Priydarshiet.al has proposed a new high speed low power dynamic circuit design technique using 20nm FinFETs. By applying the appropriate clock and sleep signal to the back gates of the FinFETs, the proposed circuit can efficiently control the dynamic power. The FinFET is the leading example of multigate MOSFETS to substitute conventional single gate MOSFETs for ultimate scaling. The FinFET structure is a combination of a thin channel region and a double gate to suppress the short channel effects (SCEs) and Vth variation . By using FinFET,figure of merits viz. ION, IOFF, output resistance, propagation delay, noise margin and leakage power, can be improved for ultra low power and high performance applications. During the pre-charging period, Vth of PMOS is controlled low so that a fast precharging can occur.

In this paper[10], Sandeep et.al has presented a research on existing clocked regenerative double-tail comparators in terms of power dissipation, PDP (power-delay product) and slew-rate. Based on the simulation results, a new comparator with two stage signaling is presented for low-power dissipation and high performance. The low voltage clocked regenerative comparator provides maximum speed and power efficiency and is thus required for implementing area efficient and ultra low-power analogue to digital converters (ADCs). For an analog and mixed signal design, comparator is the main component in low-power applications. Clocked regenerative comparators have features like zero static power dissipation, high input impedance for better transconductance, good strength against noise and low offset voltage. The simulation result at 90nm CMOS technology approves the research purpose. This states that in proposed comparator, the power consumption is considerably reduced at 1.2Vsupply.

In [11] , Sujata et.al has shown the analysis of Double Tail Comparator according to its dynamic power, static power and leakage current. From the analysis of Double Tail Comparator, a new design is proposed which is a modification of Conventional Double Tail Comparator for very small power, small voltage and high speed operation. They have used Tanner EDA software for designing these comparators with 180 nm technology. Then, they have compared the results of both of these comparators. It is shown that from the proposed structure of Double Tail Comparator, the leakage current, static power and dynamic power are significantly reduced. For the supply voltage of 0.8 V, the proposed comparator consumes reduced power of 22.3054 nW and current of 27.8818 nA.

In paper[12] ,Parvin et.al has presented a new ultra-low power double-tail latched comparator suited for biomedical applications. The proposed comparator benefits from a positive feedback to achieve high resolution with low kickback noise. It is shown by time analysis and simulation that the delay time is significantly reduced compared to a conventional double-tail latched comparator. The presented circuit is designed and simulated in 0.18-lm CMOS technology. The post-layout simulation results show that the designed comparator consumes only 1.56 nW power, at 600 mV supply voltage and 100 kHz clock frequency. This amount is 54.35 % of power consumption of a conventional double-tail latched comparator with the same input referred offset of 7.5 mV. Furthermore, the proposed circuit provides a self-neutralization technique which results 8.8 % reduction of kick-back noise in comparison to the conventional latched comparator. The maximum clock frequency of this circuit is 200 MHz at 1 V supply voltage. The proposed circuit as a power-delay product of 0.0172 fJ at 100 kHz clock frequency. The proposed comparator is well designed to operate with supply voltages between 400 mV and 1 V.

In [13] , Abhishek et.al has designed the circuits using 0.18µm CMOS technology with 1.8v bias voltage and 1-2µA bias current. This paper also discusses the advantage of using programmable hysteresis to the comparators. Tanner EDA environment is used for the design and simulation for the comparator circuits. Comparison of the proposed comparator with existing double tail comparator is performed and the result is discussed in detail. Basically,the fast-growing electronics industry is pushing towards high speed low power analog to digital converters. Comparator is electronic devices which are mainly used in Analog to Digital converter (ADC). In ADC they are used for quantization process, and are mainly responsible for the delay produced and power consumed by an ADC. A high speed low power comparator is required to satisfy the future demands.

In [14], Monica et.al has designed a new double tail comparator, where the circuit of a conventional double tail comparator is modified for low power and fast operation even in small supply voltages. Without complicating the design and by adding few transistors the positive feedback during the regeneration is strengthened which results in remarkably reduced delay time. Post layout simulation results in a 0.18µm technology confirm the analysis results. It is shown that in the switching transistors using dynamic comparator, both the power consumption and delay time are significantly reduced. Power consumption of conventional double tail comparator is 12µW in 0.8v and power is reduced to 9.5µW in double tail comparator using switching transistors with the same supply voltage.

In paper [15], Dharmendra et.al has basically described the comparator circuits used in FLASH Analog to digital converter (ADC). The performance of FLASH ADC is greatly influenced by the choice of comparator. In this paper, first a single ended "Threshold Inverter Quantizer" (TIQ) is presented. The TIQ comparator is based on a CMOS inverter cell, in which voltage transfer characteristics (VTC) are changed by systematic transistor sizing. However, TIQ comparator is very sensitive to power supply noise. Another comparator circuit presented in this paper is "Two stage open loop comparator". It is implemented in 50 nm CMOS Technology. Pre-simulation of comparator is done in LT-Spice and post layout simulation is done in Microwind 3.1. This architecture can be extended to medium-to-high resolution applications because the simplicity of the circuit. Comparator is a main part of flash ADC.

In this paper [16], Deepak et.al has done an analysis on the delay and power of the dynamic comparators and based on the presented analysis, a new dynamic comparator has been proposed, in which the conventional double tail comparator is modified for low power and fast operation even in small supply voltages. Here by adding a few transistors, the power consumptions can be reduced drastically. The need of analog to digital converters with ultra low power, area efficient and high speed is giving more chance to the use of dynamic regenerative comparators to maximize the speed and power efficiency. Based on the analysis, a new dynamic double tail comparator with low voltage, low power capability was proposed to improve the performance of comparator, mainly concerned in power consumption. Post–layout simulation using 180nm CMOS technology confirms the analysis results of the proposed dynamic comparator.

In [17], Kale et.al has reported comparator design for low power & high speed. The present Design is specially design for high resolution Sigma Delta Analog to Digital Converters (SDADCs). Design is based on two stage CMOS OP-AMP technique. Simulation results have been obtained by 0.5-

micron technology, considering ±2.5 supply voltage & 2.5 V Input range. Design has been carried out in Tanner tool using HP 0.5-micron technology. Simulation results are verified using S-Edit and W-Edit. They have achieved the propagation delay (speed) of 3.6 nano sec. with low power consumption about 0.31 mW. Design has used the two stage CMOS OPAMP design technique generally it referred as a open loop comparator where we eliminate the compensation to achieved better performance. Finally, they have compared the proposed results with earlier work done and get improvement in presented results

VI. PROPOSED SYSTEM

The simulated waveform of the proposed comparator are shown in Figure 5. The circuit is designed and simulated with TANNER EDA using 180nm technology file and the design and simulation conditions are VDD=1.8VTherefore, the proposed comparator provides better input offset characteristic and faster operation in addition to the advantages of those comparators such as less kickback noise, reduced clock load and removal of the timing requirement between CLK and CLK' over a wide common-mode and supply voltage range. For its operation, during the reset phase, when CLK=0,M-tail1 &M-tail2 are off, M3 & M4 transistors gets on and charge the fp and fn nodes to Vdd, during this time Mc1 & Mc2 transistors are cut off. then Mr1 & Mr2 intermediate transistors reset latch output to ground.

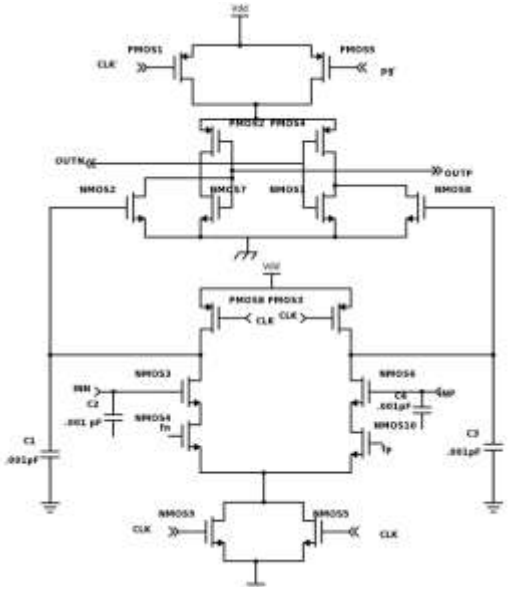

Fig 5: Schematic of Proposed Comparator

VII. CONCLUSION

A novel low power consumption, low offset and high-speed dynamic latched comparator has been proposed in this research work. The gain was improved by inserting two additional inverters between input and output stage. The comparator action depends upon various factors like power supply, technology area etc. However, of various things our aim is to achieve a low power design so compromise with other factors is to be made. Also, this paper provides a brief analysis on different types of comparators and their performance analysis. The comparator will be designed using Tanner EDA using 180 nm technology file. Simulations will be carried out on different comparator to obtain the best results. Power and speed are the major areas of concern. Moreover, With the literature review we have done so far, we can say that the double-tail dual-rail latch comparator which has a back to back latch stage has the lowest power dissipation. Dynamic comparators have less dynamic power dissipation and input offset voltage compared to the pre-amplifier based comparator. But their speed is the latter due to the parasitic capacitances.

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